Connecting the DECchip 21040 Ethernet LAN Controller to the Network: An Application Note

Order Number: EC–QE4MA–TE

This application note provides information necessary to implement network connections to the DECchip 21040 Ethernet LAN controller. Connections can be made to CPUs with a direct connection to an onboard peripheral component interconnect (PCI) local bus, or to CPUs without a direct PCI connection by using a bus-to-bus interface.

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Overview

This application note describes how to implement network connections to the DECchip 21040 Ethernet LAN controller (21040). Its primary objective is to achieve an error-free implementation of the Ethernet network interface. This application note describes only hardware implementations by providing hardware designs and layout rules.

For detailed technical product requirements, the product developer should refer to the *DECchip 21040 Ethernet LAN Controller for PCI Data Sheet* and the *DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual*.

Functional Overview

This section provides an overview of the system and network interfaces.

System Interface

The 21040 has a single 50-pin connection, which consists of the control and address/data signals of a PCI bus.

The 21040 provides complete implementation of the IEEE 802.3 Ethernet specification from the attachment unit interface (AUI) and the twisted-pair (10BASE-T) interface through the media access control (MAC) layer, and creates a direct interface to the PCI bus. The PCI board operates on the bus and uses only 1% of the bus bandwidth during an Ethernet reception or transmission. The bus master design provides for high throughput between the system and the network, yet it requires only a minimum of parts for a complete implementation.

Network Interface

The 21040 physical layer design supports AUI drop cable Ethernet and 10BASE-T twisted-pair (TP) Ethernet connections. AUI_TP, pin 76, is used to select the AUI or TP interface. Connect pin 76 to 3.3 V to select AUI; connect pin 76 to ground to select TP. Pin 76 should *never* be connected to 5 V. The AUI, TP selection can also be programmed, overriding the hardware pin selection.

When the AUI port is selected, the following AUI signals can be active:

Signal	Pin Number
AUI_RD–	71
AUI_RD+	72
AUI_TD–	81
AUI_TD+	82
AUI_CD–	74
AUI_CD+	75

These signals interface with the Manchester encoder/decoder portion of the 21040. The 21040 supports 10BASE2 thickwire and 10BASE5 ThinWire connections.

When the 10BASE-T port is selected, the following TP signals can be active:

Signal	Pin Number
TP_RD–	77
TP_RD+	78
TP_TD+ +	85
TP_TD–	86
TP_TD+	87
TP_TD– –	88

These signals interface with the Manchester encoder/decoder portion of the 21040.

Note

Only one interface can be active at a time.

Physical Layer

The physical layer of the 21040 can be used in AUI or 10BASE-T configurations. Different methods are used to connect each port to the actual cable connector.

10BASE-T Twisted-Pair Network Port

Figure 1 and Figure 2 show the physical layer design for 10BASE-T connection. The principal difference between the two configurations is the driver and the transformer module. The driver can be replaced with a transformer module. The filter and transformer components minimize any potential electromagnetic interference and radio frequency interface problems. Common-mode noise (when noise between two lines of the same polarity, add rather than cancel) can radiate energy from the TP interface. Also, significant common-mode power supply noise can be generated on the board or adapter by other devices. Therefore, the use of filter and transformer modules that incorporate common-mode chokes is recommended.

Figure 1 shows the 10BASE-T network connection *with* buffers. The required components for this configuration are as follows:

- A voltage swing compensator
- Terminating and decoupling components
- A filter
- An RJ45 connector

Figure 1 10BASE-T Network Connection

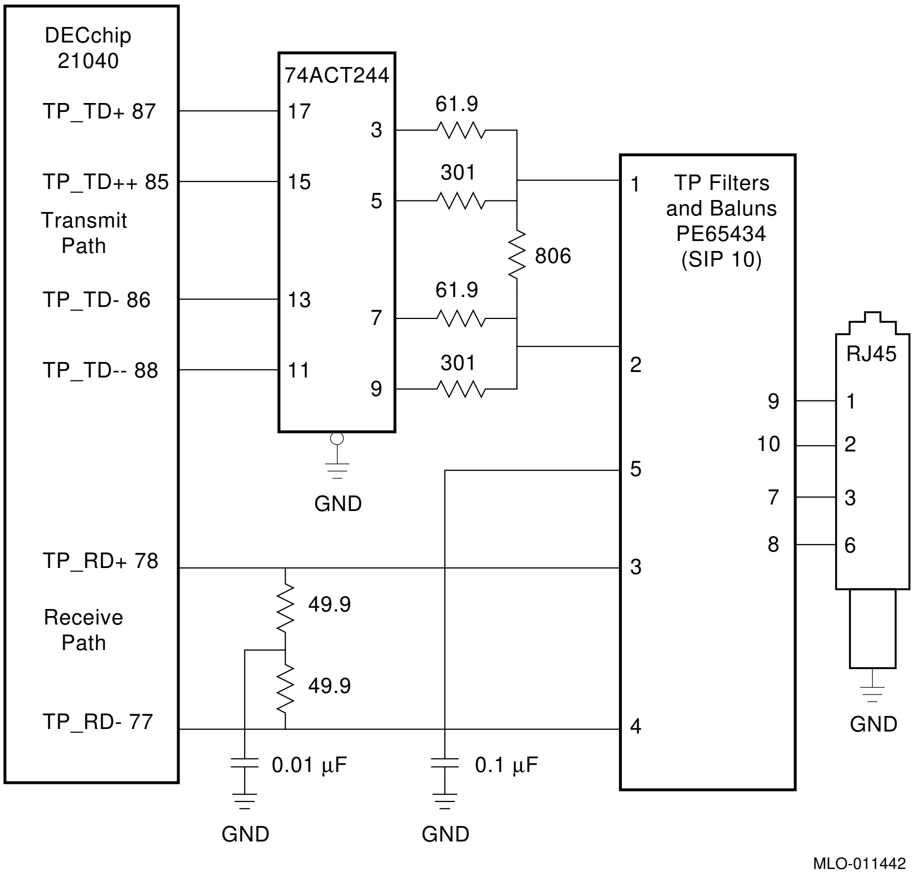
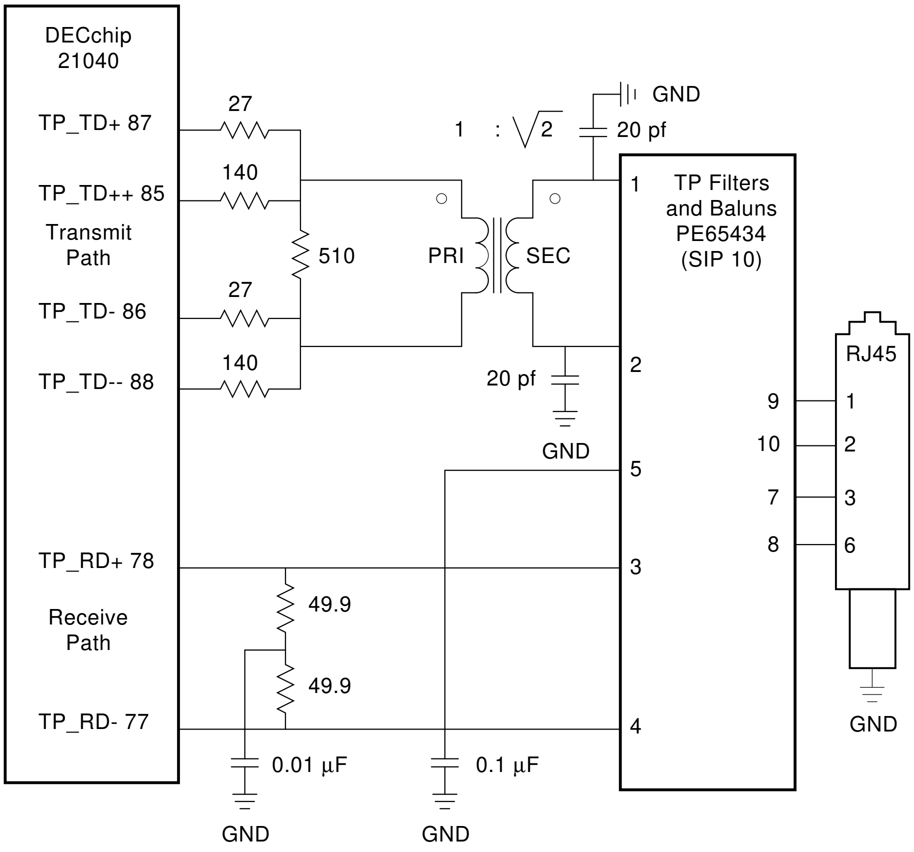


Figure 2 shows the 10BASE-T network connection *without* buffers. The required components for this configuration are as follows:

- Terminating and decoupling components
- A transformer module (ratio of 1:1.414)
- A filter
- An RJ45 connector

Figure 2 10BASE-T Network Connection Without Buffers



The Pulse Engineering PE65434 SIP 10 filter and 1:1.414 transformer can be replaced with a new single device from Pulse Engineering called PE68016. PE68016 combines both the 1:1.414 transformer and filter in one device.

AUI Network Port

The 21040 supports a fully compliant AUI. The AUI can interface with an external medium-attachment unit and connect to alternative media, such as 10BASE2 (ThinWire) and 10BASE5 (thickwire). Figure 3, Figure 4, and Figure 5 show the required connections.

Figure 3 shows the AUI 10BASE5 network connection and the pin connections between the DECchip 21040 and the isolation transformer. The required components for this configuration are as follows:

- Terminating and decoupling components
- An isolation transformer
- An AUI connector

Figure 3 AUI 10BASE5 Network Connection

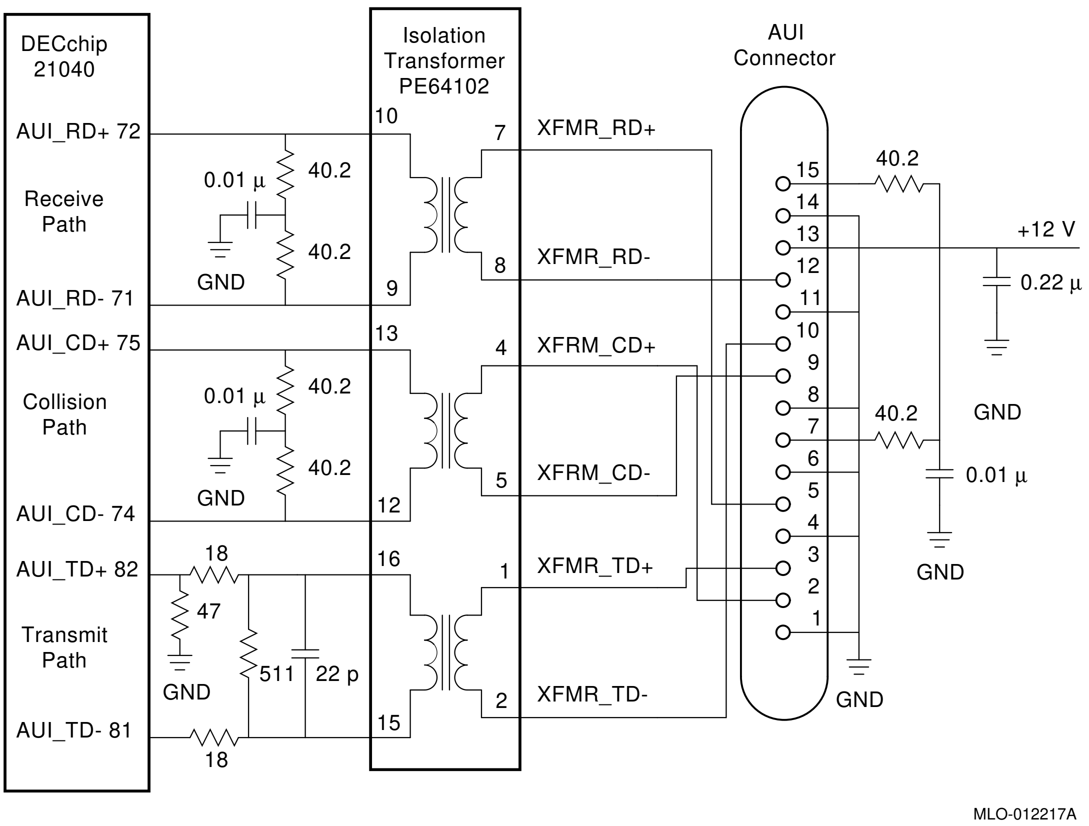
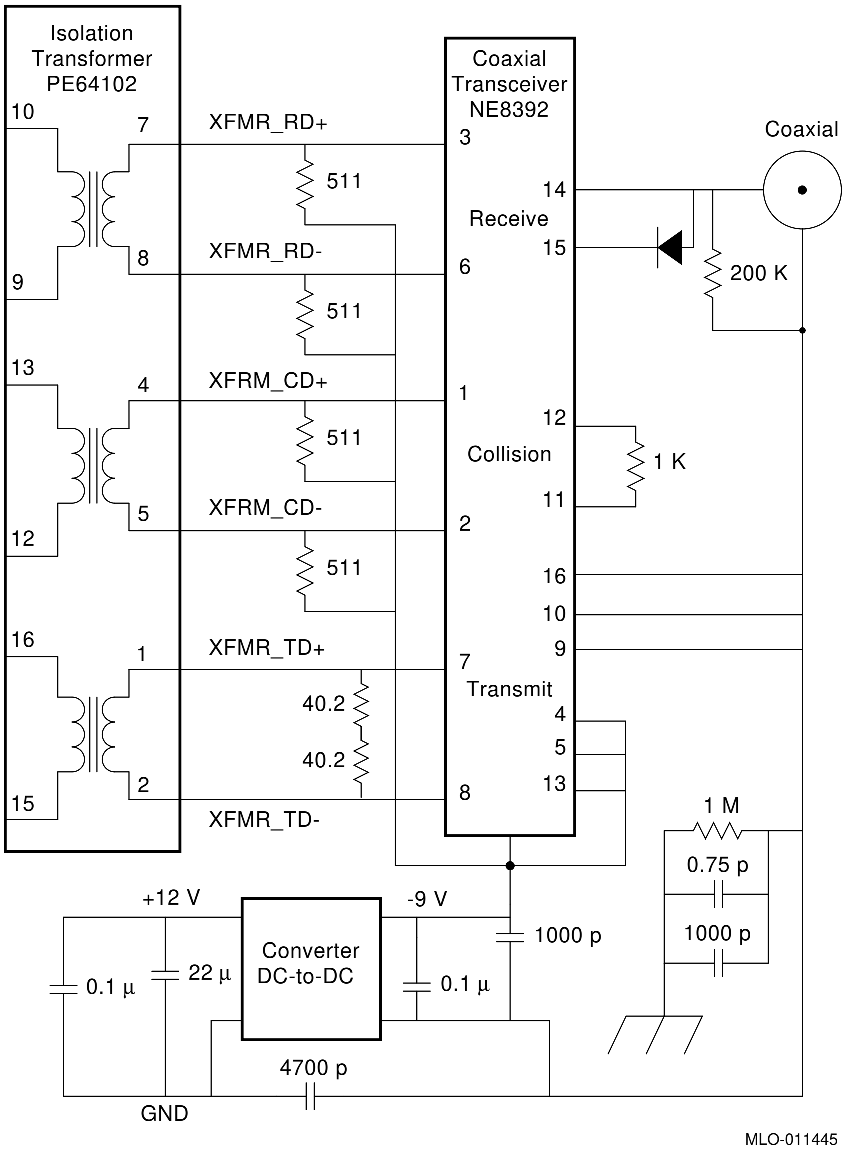


Figure 4 shows the AUI 10BASE2 network connection. In this configuration, the AUI is not externally exposed. The required components for this configuration are as follows:

- An isolation transformer
- Terminating and decoupling components
- A dc-to-dc converter
- A coaxial transceiver
- A BNC connector

Figure 4 AUI 10BASE2 Network Connection



In cases where the 10BASE2 medium-attachment unit is a separate module from the board, the medium-attachment unit can be implemented on a small add-in card. This card is mounted by a bracket on the board. Ensure that the cable used to connect the board to the medium-attachment unit provides adequate shielding of the AUI signals from external noise.

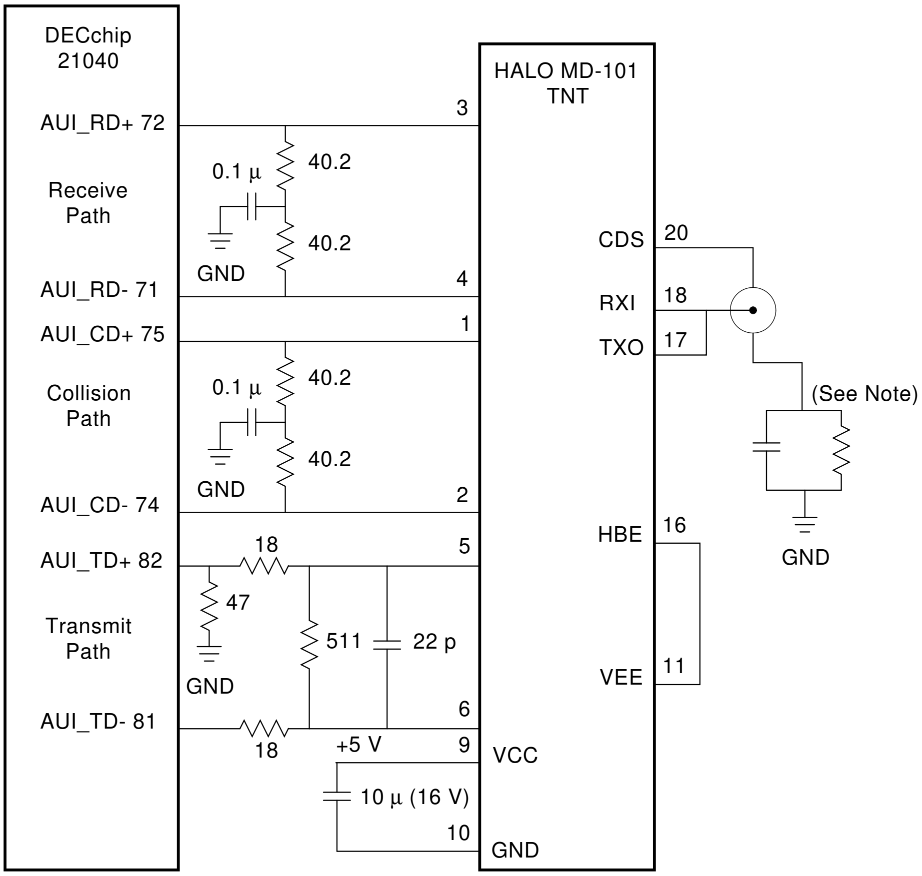
This medium-attachment unit connection includes the following components:

- A transceiver chip
- A BNC connector
- A dc-to-dc converter
- Discrete devices, resistors, capacitors, and so on

Figure 5 shows the AUI 10BASE2 network connection with a Thin Net Transceiver (TNT). The required components for this configuration are as follows:

- Termination and decoupling components
- A TNT transceiver
- A BNC connector

Figure 5 AUI 10BASE2 Network Connection with Thin Net Transceiver (TNT)



Note: 1 M ohm 750 V resistor and 0.01 uF 500 VAC rms for static discharges and safety considerations.

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Implementing Network Connections

Layout Considerations

The 21040 implements the functions of an Ethernet node controller, a serial interface adapter, a 10BASE-T transceiver, and an industry-standard PCI bus on the board. Only a few tasks are necessary to complete an Ethernet design.

However, you must adhere to requirements for electromagnetic and radio-frequency interference. Any noise capacitively coupled to the 21040 could be transmitted over the network. If this occurs, then the network media becomes an antenna and radiates high-frequency noise. Therefore, the Ethernet circuitry must be isolated from noise.

Signal Routing and Placement

The Ethernet circuitry should be kept free of interference from unrelated signal traces. Routing for other signals must be kept away from the space surrounding the grouped Ethernet components. Place the Ethernet circuitry at the perimeter of the board, as near to the corner of the board and the 21040 as possible. That is, pin number 1 of the 21040 would be located in the lower right-hand corner as shown in Figure 6.

The 21040 and the crystal oscillator house critical timing mechanisms, which are also sensitive to noise. Place other noisy devices, such as the CPU and system clock, away from these components.

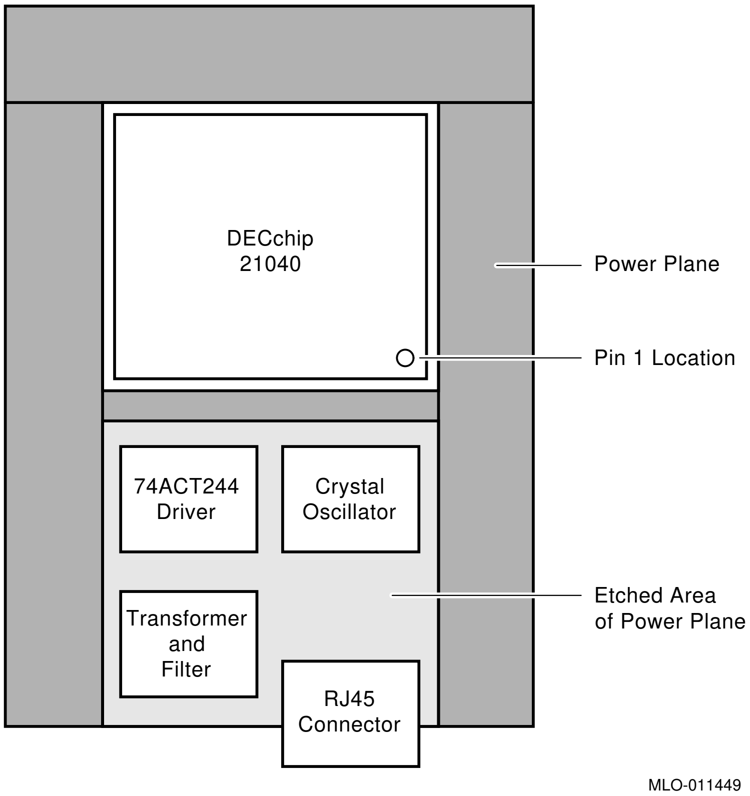
Keep all signal paths short and route them as directly as possible. Systems using the 10BASE-T nodes can be connected by cables up to 100 m. As a result, the signal that reaches the board can be noisy and low in amplitude. To minimize corrupting this data, route these signals, by the most direct path, from the system's physical connector to the transceiver and the 21040. The length of this path should not exceed 8 cm (3 in) for the following receive data signals:

Signal	Pin Number
AUI_RD–	71
AUI_RD+	72
AUI_CD–	74
AUI_CD+	75
TP_RD–	77
TP_RD+	78

Ground and Power Planes

When the Ethernet devices are in place, isolate them from noise within the ground and power planes. Because the ground plane is not etched, isolate noise by etching the power plane. Power-layer etching is accomplished by creating noise fences around some areas and noise-free islands beneath other areas. Figure 6 shows a power and ground plane etching scheme.

Figure 6 Power and Ground Plane Etching Scheme



Create an etch in the power plane that almost completely surrounds the Ethernet component group. The opening in this barrier should be oriented in a way that prevents noise produced by the rest of the board from having a straight path into the isolated area. This fence-type barrier effectively prevents noise on the 21040 board from being transmitted to the network.

The following table shows the media-specific interface components for 10BASE-T access:

Access Type	Components	Functions	Available Part Numbers
10BASE-T	74ACT244 driver	Voltage-swing compensators	74ACT244 or 74FCT244
	Filter and transformer module	$1{:}\sqrt{2}$	Pulse Engineering PE65745 (SMD[1]), Valor PT4096 (SMD[1]), Valor ST7011 (SMD[1]), Halo TD42-2006Q (SMD[1]), or Halo TG42-2006W1 (SMD[1])
	Transformer filter and chokes	Magnetics	Pulse Engineering PE65434 or Valor FL1012
	RJ45 wire jack connector	—	—

[1]Surface mount device

The following table shows the media-specific interface components for 10BASE2 and 10BASE5 access:

Access Type	Components	Functions	Available Part Numbers
10BASE2	dc-to-dc converter	—	—
	Isolation transformer	—	Pulse Engineering PE64102 (SMD[1]), Pulse Engineering PE65723 (SMD[1]), Valor LT6032 (SMD[1]), Valor ST6032/3 (SMD[1]), Halo TD01-0756K (SMD[1]), or Halo TG01-0756W (SMD[1])
	Transceiver	Coaxial	National DP8392C
	Connector	Coaxial	—
10BASE5	Isolation transformer	—	Pulse Engineering PE64102 (SMD[1]),
		—	Pulse Engineering PE65723 (SMD[1]),
		—	Valor LT6032 (SMD[1]),
		—	Valor ST6032/3 (SMD[1]),
		—	Halo TD01-0756K (SMD[1]), or
		—	Halo TG01-0756W (SMD[1])
	AUI connector	D type—15 pins	—

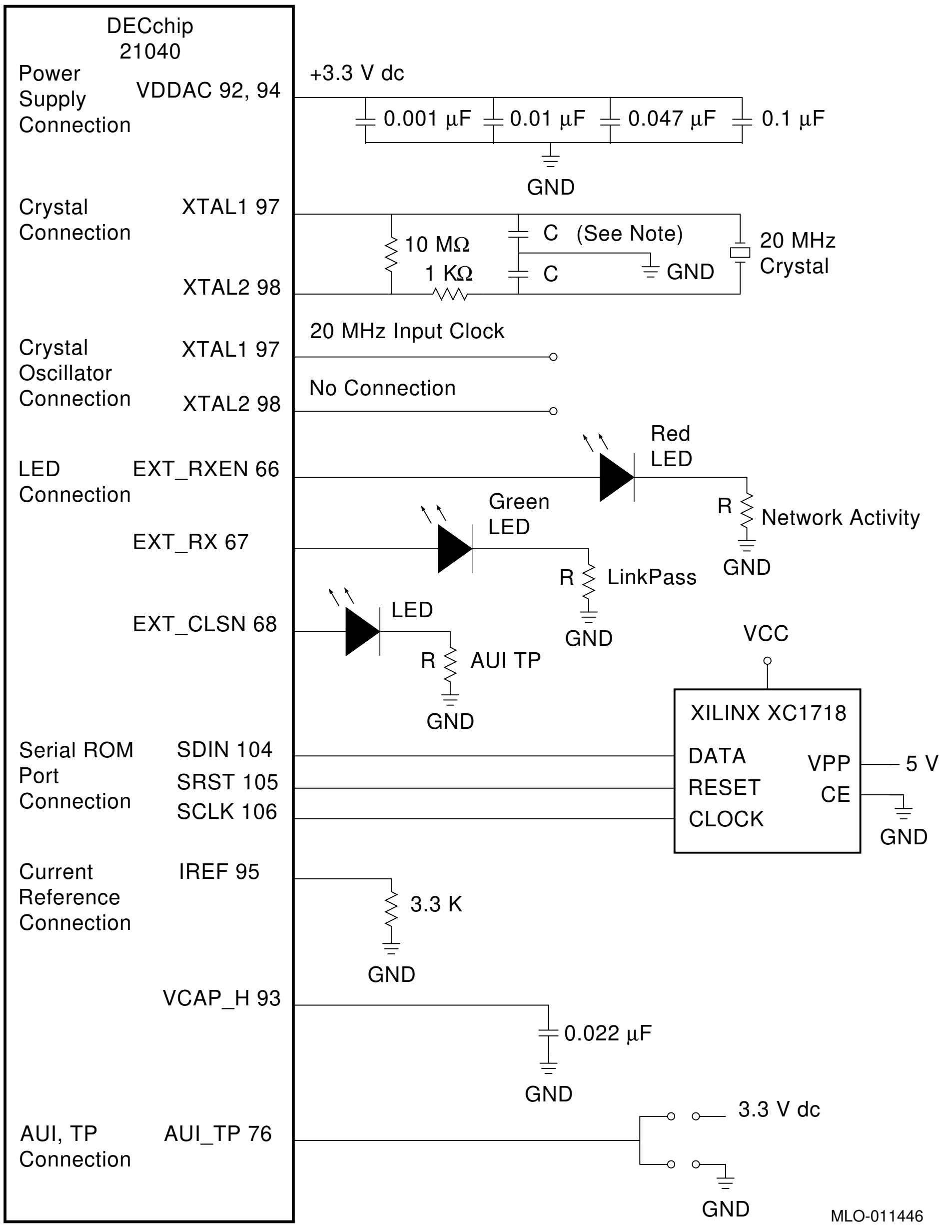
[1]Surface mount device

3.3-V Power Supply

The 21040 operates with a power supply of 3.3 V. Four decoupling capacitors are recommended: 0.1, 0.01, 0.001, and 0.047 (all values are in microfarads). Because of the 21040 architecture, all analog functionality is contained on one corner of the 21040.

Figure 7 shows the DECchip 21040 signal connections.

Figure 7 DECchip 21040 Signal Connections



Implementing Network Connections

Crystal and Crystal Oscillator Connections

Figure 7 shows two serial clock connections; select either the crystal connection or crystal oscillator connection.

Use a crystal that implements only the Ethernet timing circuitry. (The standard for Ethernet connections is a 20-MHz crystal.) The crystal must not vary by more than 100 parts per million (PPM), or 0.01%. Place the crystal as close as possible to the 21040.

Because the frequency of crystals from different vendors can vary, test the crystals in the actual circuit. It might be necessary to vary the tuning of the surrounding capacitors. However, after the capacitors have been tuned for the specific crystal, the design does not need to be altered on a board-by-board basis.

The 21040 also supports a crystal oscillator input (Figure 7), thus eliminating the need for surrounding capacitors. This is useful for applications with multiple network connections to Ethernet connections.

LED Status Signals

The 21040 supports the following three LED status signals (see Figure 7):

- Network Activity—This LED is driven from EXT_RXEN, pin 66. The network activity LED is on when any activity on the network is sensed.
- LinkPass/LinkFail—This LED is driven from EXT_RX, pin 64. The LinkPass/LinkFail LED is on when LinkPass is established.
- AUI/TP—This LED is driven from EXT_CLSN, pin 68. The AUI/TP LED is on when the attachment unit interface is selected. When this LED is off, the twisted-pair interface is selected.

Note

In Figure 7, the value of the pull-up resistor (R) depends on the rating of the LED used.

Serial ROM Port

The serial ROM port is programmed with the Ethernet ID. Each Ethernet adapter must have a unique Ethernet ID number. The serial ROM signals include the following (Figure 7):

- Serial ROM data in—This signal is driven from SDIN, pin 104. The ROM data output is used to drive SDIN.
- Serial ROM reset—This signal is driven from SRST, pin 105. When this signal is deasserted, it enables the data output driver. When this signal is asserted, both the internal address and bit counters are reset.
- Serial ROM clock—This signal is driven from SCLK, pin 106. The ROM clock signal clocks internal address and bit counters to read the configuration programs.

If the serial ROM port is not used, then SDIN should remain grounded, and SRST and SCLK should not be connected.

Other Considerations

The host driver must set the default configuration after reset to either pin_configuration or auto_configuration. In pin_configuration, the AUI port or the 10BASE-T port is configured depending on the state of the AUI_TP, pin 76 (Figure 7). In auto_configuration, the configuration is programmed by the contents of control and status register CSR13.

The current reference input (IREF, pin 95) for the analog phase-locked loop (PLL) logic is connected by a 3.3-kΩ resistor to ground. In addition, the capacitor (VCAP_H, pin 93) is connected by a 0.022-μF capacitor to ground (see Figure 7).

Add 5-kΩ pull-up resistors from TMS (pin 60) to Vdd and from TDI (pin 59) to Vdd. If the JTAG port is unused, connect TCK (pin 61) to ground, and do not connect TDO (pin 57).

Technical Support and Ordering Information

This section describes how to obtain information and technical support, and how to order products and associated literature.

Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

Ordering Digital Semiconductor Products

To order Digital Semiconductor samples or Sample Kits call **1–800–DIGITAL**.

To order the DECchip 21040 Ethernet LAN Controller for PCI or the DECchip 21040 Evaluation Board Kit, contact your local distributor.

You can order the following semiconductor products from Digital:

Product	Order Number
DECchip 21040 Ethernet LAN Controller for PCI	21040–AA
DECchip 21040 Evaluation Board Kit	21A40–01

Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature related to the DECchip 21040 Ethernet LAN Controller for PCI. For a complete list, contact the Digital Semiconductor Information Line. For ordering information, see the Ordering Electronically and Ordering by Telephone and Through Direct Mail sections.

Title	Order Number
Alpha Architecture Reference Manual[1]	EY–L520E–DP–YCH
DECchip 21040 Ethernet LAN Controller for PCI Product Brief	EC–N0281–72
DECchip 21040 Ethernet LAN Controller for PCI Data Sheet	EC–N0280–72
DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual	EC–N0752–72
DECchip 21040 PCI Evaluation Board User's Guide	EC–N0753–72
Ethernet Address ROM Programming: An Application Note	EC–N3214-72

[1]To order and purchase the *Alpha Architecture Reference Manual*, call **1–800–DIGITAL** from the U.S. or Canada, or contact your local Digital office, or technical or reference bookstore where Digital Press books are distributed by Prentice Hall.

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI System Design Guide	PCI Special Interest Group N/S HH3–15A 5200 N.E. Elam Young Pkwy Hillsboro, Oregon 97124–6497 503–696–2000

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