Digital Semiconductor

Alpha 21164 Microprocessor

Product Brief

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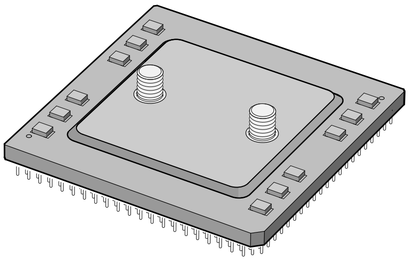

Description

The Alpha 21164 microprocessor is a high-performance implementation of Digital's Alpha architecture designed for application servers and high-performance clients. It has a superscalar design capable of issuing four instructions every clock cycle. The integration of an instruction cache, data cache, and second-level cache offers unrivaled microprocessor performance. The 21164 uses a high-performance interface to access main memory, data buses, and an optional board-level cache.

Features

- Fully pipelined 64-bit advanced RISC (reduced instruction set computing) architecture supports multiple operating systems, including:
  - Microsoft Windows NT
  - Digital UNIX
  - OpenVMS
- Best-in-class performance
  - 266 through 300 MHz operation
  - 290 through 330 SPECint (est.)
  - 440 through 500 SPECfp (est.)
  - Superscalar (4-way instruction issue)
  - Peak instruction execution rate of over 1200 million instructions per second
  - 0.50 μm CMOS technology
- Pipelined (9-stage) floating-point unit
  - IEEE single- and double-precision operation
  - VAX F_floating and G_floating data types
  - Longword and quadword data types
- Pipelined (7-stage) integer unit
- Memory-management unit
  - Demand-paged memory management
  - 48-entry, fully associative instruction translation buffer
  - 64-entry, fully associative data translation buffer
  - Each translation buffer entry able to map 1, 8, 64, or 512 8KB pages; each entry supports all four granularity hint bit combinations
- Onchip, 8KB, direct-mapped, write-through L1 data cache
- Onchip, 8KB, direct-mapped L1 instruction cache
- Onchip, 96KB, 3-way, set-associative write-back L2 unified instruction and data cache
- Onchip write buffer with six fully associative 32-byte entries
- High-performance interface
  - 128-bit memory data path
  - Selectable error correction code (ECC) or parity protection on data
  - 40-bit addressing
  - Programmable interface timing
  - Two outstanding load instructions
  - Control for optional offchip L3 cache
  - Synchronous/asynchronous RAM support
  - Programmable cache block size
  - Programmable cache speed, one-third to one-fifteenth of clock speed
- Programmable performance counters to measure CPU and system performance
- Serial ROM interface
  - Loads instruction cache after reset
  - Allows software-controlled serial port after initialization
- Chip- and module-level test supports JTAG (IEEE 1149.1)
- 3.3-V I/O supply voltage with chip interface directly to 5-V logic
- 499-pin ceramic interstitial pin grid array (IPGA) package
- Privileged architecture library code (PALcode) supports
  - Optimization for multiple operating systems
  - Flexible memory-management implementations
  - Multi-instruction atomic sequences

Alpha 21164 Microarchitecture

The 21164 microprocessor consists of five independent functional units: the instruction fetch, decode, and branch unit; the integer execution unit; the memory-management unit; the cache control and bus interface unit; and the floating-point unit. There are three onchip caches: the instruction cache, the data cache, and the second-level cache.

Pipeline Organization —The microprocessor uses a 7-stage pipeline for integer operate and memory reference instructions. It uses a 9-stage pipeline for floating-point operate instructions. The instruction unit maintains state for all pipeline stages to track outstanding register write transactions.

Instruction Fetch, Decode, and Branch Unit —The instruction unit fetches, decodes, and issues instructions to the integer unit, memory-management unit, and floating-point unit. It manages the pipelines, the program counter (PC), the instruction cache, prefetching, and instruction stream memory management. The instruction unit can decode up to four instructions in parallel and check that required resources are available for each.

Integer Execution Unit —The integer execution unit contains two 64-bit integer pipelines. Results of most integer operations are available for use by subsequent instructions. The integer unit also partially executes all memory instructions by calculating the effective address.

Memory-Management Unit —The memory-management unit processes all load and store instructions; two load instructions can be executed in parallel. (The data cache is dual ported to support this.) Up to 21 load instructions can be in progress at any time. The memory-management unit also manages the data cache and logic that serializes and merges load instructions that miss the data cache.

Cache Control and Bus Interface Unit —The cache control and bus interface unit processes all accesses sent by the memory-management unit and implements all memory-related external interface functions. The cache control and bus interface unit also manages all cache coherence protocol functions. It controls the L2 cache and the optional offchip L3 cache.

Floating-Point Unit —The floating-point unit contains a floating-point multiply pipeline and a floating-point add pipeline. (Divides are associated with the add pipeline but are not pipelined themselves.) IEEE S_ and T_floating data types are supported with all rounding modes. VAX F_floating and G_ floating data types are fully supported. VAX D_floating data types are partially supported.

Instruction Cache —The instruction cache is an 8KB virtual direct-mapped cache with 32-byte blocks.

Data Cache —The data cache is a dual-ported, 8KB, write-through, read-allocate, direct-mapped, physically addressed cache with 32-byte blocks.

L2 Cache —The onchip L2 cache is a 96KB, 3-way, set-associative, physical, write-back, write-allocate, data and instruction cache. The cache is fully pipelined and supports both 32-byte and 64-byte blocks.

Optional Offchip L3 Cache —The 21164 supports and fully manages a direct-mapped external backup cache (optional). This cache is a physical, write-back, write-allocate cache with 32-byte or 64-byte blocks. The L3 cache controller supports synchronous and asynchronous cache RAMs. Wave pipelining can be used with asynchronous RAMs in the 64-byte block mode. It is a mixed data and instruction cache. The user can select an L3 cache size of 1, 2, 4, 8, 16, 32, or 64MB.

Big Endian Support —The 21164 provides limited support for big endian data formats. One mode inverts physical bit <2> for all longword references. Another mode complements operand Rbr <2:0> on EXTxy, INSxy and MSKxy instructions.

Virtual Address Space —The virtual address is a 64-bit unsigned integer that specifies a byte location in the virtual address space. The microprocessor implements a 43-bit subset of the virtual address space and supports a 40-bit, 1-terabyte physical address space.

Thermal Management

The 21164 dissipates approximately 50 watts. Conventional forced air cooling methods are sufficient to remove heat and maintain the highest levels of reliability. The user may also define an application-specific heat sink. Digital specifies two separate heat sinks for this device. Both are specified to 1000 LFM. One heat sink has mounting holes in line with the cooling fins and is approximately $6.6 \times 6.6 \times 3.3$ cm ($2.6 \times 2.6 \times 1.3$ in). The other heat sink has mounting holes rotated 90 degrees from the cooling fins and measures approximately $7.6 \times 7.6 \times 4.6$ cm ($3 \times 3 \times 1.8$ in).

Alpha Architecture Summary

As implemented in the 21164, the Alpha architecture supports:

- A fixed 32-bit instruction size
- Separate integer and floating-point registers
  - Thirty-two 64-bit integer registers
  - Thirty-two 64-bit floating-point registers
- 32-bit (longword) and 64-bit (quadword) integer data types
- 32-bit and 64-bit IEEE and VAX floating-point data types
- Memory accesses, using a 64-bit virtual byte address
- Privileged architecture library code (PALcode)

Instruction Set

All instructions are 32 bits long and use one of four different instruction formats. Each format uses a 6-bit opcode and zero, one, two, or three 5-bit register fields.

CALL_PAL Instructions — These instructions vector to a privileged layer of software that atomically performs both privileged and unprivileged functions.

Branch Instructions — Conditional branch instructions test a register for positive/negative, zero/non-zero, or even/odd, and perform a PC-relative branch. Unconditional branch instructions perform either an absolute or PC-relative jump, using an arbitrary 64-bit register value. Unconditional branch instructions can update a destination register with a return value.

Load/Store Instructions — These instructions can move either 32-bit or 64-bit quantities. Eight-bit and 16-bit load/store operations are supported through an extensive set of in-register byte manipulations. The I/O bus directly supports byte and word operations in hardware.

Operate Instructions — Integer operate instructions manipulate full 64-bit values and include a full complement of arithmetic, compare, logical, and shift instructions. There are also three 32-bit integer operates: add, subtract, and multiply.

In addition to conventional RISC operation, the instruction set provides scaled add/subtract for quick subscript calculation; 128-bit multiply for multiprecision arithmetic and division by a constant; conditional moves for avoiding branches; and an extensive set of in-register byte manipulation instructions.

Floating-point operate instructions include four complete sets of instructions for IEEE single-precision, IEEE double-precision, VAX F_floating, and VAX G_floating arithmetic. In addition to arithmetic instructions, there are instructions for conversions between floating and integer values, including the VAX D_floating data type.

PALcode

PALcode is a privileged layer of software that automatically performs such functions as the dispatching and servicing of interrupts, exceptions, task switching, and additional privileged and unprivileged user instructions as specified by operating systems using the CALL_PAL instruction.

PALcode is the only method of performing some operations on the hardware. In addition to the instructions defined by the Alpha architecture, a set of implementation-specific instructions is provided.

PALcode runs in an environment with privileges enabled, instruction stream mapping disabled, and interrupts disabled. Disabling memory mapping allows PALcode to support functions such as TB-miss routines. Disabling interrupts allows the instruction stream to provide multi-instruction sequences as atomic operations.

Memory Management

The memory-management architecture provides:

- A large address space for instructions and data
- Convenient and efficient sharing of instructions and data
- Independent read and write access protection
- Flexibility through programmable PALcode support

Alpha Architecture Compared to Conventional RISC Architecture

Feature	Alpha Architecture Difference
64-bit architecture	A true 64-bit architecture with 64-bit data and address — not a 32-bit architecture expanded to 64 bits.
High speed	Suited to very high speed implementations. All instructions are simple and 32 bits in length. Memory operations are either load or store instructions. All data manipulation is done between registers. There are no implementation-specific pipeline timing hazards, no load delay slots, and no branch delay slots.
Multiple operating systems	The user can implement a privileged layer of software (PALcode) for operations specific to an operating system. This allows the processor to run OpenVMS by using one version of the privileged software, run OSF/1 by using a second version, or run Microsoft Windows NT by using a third version. Additional operating system implementations can be efficiently supported.
String manipulation	The Alpha architecture has a powerful set of instructions that support dramatic performance improvements in string manipulation. These instructions allow string manipulation to take place in-register 8 bytes at a time. Using these instructions eliminates performance penalties of an 8-byte memory transfer required in other RISC architectures.
Optimized arithmetic performance	The Alpha architecture provides the programmer with flexibility in optimizing arithmetic performance. Most conventional RISC processors require precise exception handling for arithmetic traps. This creates inherent bottlenecks in program execution. With Alpha, exceptions are imprecise by default, improving arithmetic performance. The programmer can select precise exceptions by using the trap barrier instruction.
HINTS	A number of implementation-specific HINTS are included for higher performance. Software can provide HINTS to the hardware for optimum operation. HINTS can help improve use of the pipeline, cache memory, and translation lookaside buffers.

Characteristics	
Characteristic	**Specification**
Power supply	Vss 0.0 V, Vdd 3.3 V ± 5%
Storage temperature range	–55°C to 125°C
Power dissipation @ Vdd = 3.45 V and Frequency = 300 MHz	50 W
Package	499-pin ceramic IPGA

For More Information

To learn more about the availability of the Alpha 21164 microprocessor, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717
1-800-332-2515 (TTY)

Outside North America, call:

+1-508-568-6868

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