# SPICE Models for Alpha Microprocessors and Peripheral Chips: An Application Note

This application note provides pin-to-model reference tables for Alpha microprocessors and peripheral chips. This application note is for design engineers who conduct Level 3 SPICE simulations of Alpha microprocessors and peripheral chips.

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**SPICE Level:** Level 3 SPICE Models

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# Contents

# Preface

This preface provides information about the purpose, audience, and structure of this document, the *SPICE Models for Alpha Microprocessors and Peripheral Chips: An Application Note*. It also describes the conventions used in this document.

## Document Purpose

This document contains pin-to-model reference tables that will assist you in cross-referencing Level 3 SPICE models with Alpha microprocessors and peripheral chips.

## Document Organization

Chapter 1 includes the following pin-to-model reference tables of Alpha microprocessor chips:

- Alpha 21064A microprocessor
- Alpha 21066 and Alpha 21068 microprocessors
- Alpha 21164 microprocessor

Chapter 2 includes the following pin-to-model reference tables of peripheral chips:

- DECchip 21030 PCI Graphics Accelerator
- DECchip 21040 PCI Ethernet LAN Controller
- DECchip 21050 PCI-to-PCI Bridge
- DECchip 21052 PCI-to-PCI Bridge
- DECchip 21071–BA chip
- DECchip 21071–CA chip
- DECchip 21071–DA chip

## Intended Audience and Prerequisites

This application note is for users who are familiar with SPICE. This document provides information for design engineers who will conduct simulations of SPICE models for the aforementioned Digital products.

## SPICE Model Description

You can use the SPICE models to simulate either *Worst Case* (WC) or *Best Case* (BC) operating conditions. The SPICE model files contain subcircuits, which provide a description of the connectivity and the parameters to be used with the model.

Most of the input pins have only one subcircuit that functions for either operating condition. However, all of the driver pins and some of the input pins have two separate driver subcircuits that correspond to the two operating conditions. Either subcircuit may be instantiated for Level 3 SPICE simulation, depending on the operating condition desired.

**Note**

See the 0README.TXT file in the evaluation board kit for more information about the file and directory structure of the SPICE models.

## Reference Table Conventions

The following conventions are used in all of the pin-to-model reference tables.

| Convention | Description |
|---|---|
| Pin Name | This indicates the name of the signal pin on the chip. |
| Pin Type | This indicates whether the pin is an input (I), output (O), open drain output (OD), or bidirectional (I/O) pin. |
| File Name of Model | This indicates the name of the SPICE model file for the pin. |
| Subcircuit names ending with WC | This indicates the *Worst Case* operating condition. |
| Subcircuit names ending with BC | This indicates the *Best Case* operating condition. |
| Extents | Extents are specified by a pair of numbers in angle brackets (<>) that are separated by a colon (:) and are inclusive. For example, bits <0:3> indicates an extent including bits 0, 1, 2, and 3. |

# 1

# Reference Tables for SPICE Models of Alpha Microprocessors

## 1.1 Alpha 21064A Microprocessor Pin-to-Model Reference Table

Table 1–1 lists all the pins and the corresponding Level 3 SPICE models to use for the Alpha 21064A microprocessor, which is used on the AlphaPC64 Evaluation Board. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 3.00 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 3.60 V with a temperature of 25°C.

**Table 1–1 Alpha 21064A Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| adr_h<33:5> | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| cAck_h<2:0> | I | I_21064A.SPI | FIN |
| check_h<27:0> | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| clkIn_h | I | C_21064A.SPI | FCLK |
| clkIn_l | I | C_21064A.SPI | FCLK |
| cont_l | I | I_21064A.SPI | FIN |
| cpuClkOut_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| cReq_h<2:0> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| cWMask_h<7:0> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| dataA_h<4:3> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| dataCEOE_h<3:0> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| dataWE_h<3:0> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| data_h<127:0> | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| dcOk_h | I | I_21064A.SPI | FIN |
| dInvReq_h<1:0> | I | I_21064A.SPI | FIN |
| dMapWE_h<1:0> | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| dOE_l | I | I_21064A.SPI | FIN |
| dRAck_h<2:0> | I | I_21064A.SPI | FIN |
| dWSel_h<1:0> | I | I_21064A.SPI | FIN |

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**Table 1–1 (Cont.) Alpha 21064A Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| eclOut_h | I | Model not provided[1] | Subcircuit not provided |
| holdReq_h | I | I_21064A.SPI | FIN |
| holdAck_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| iAdr_h<12:5> | I | I_21064A.SPI | FIN |
| icMode_h<2:0> | I | I_21064A.SPI | FIN |
| irq_h<5:0> | I | I_21064A.SPI | FIN |
| perf_cnt_h<1:0> | I | I_21064A.SPI | FIN |
| reset_l | I | I_21064A.SPI | FIN |
| sRomClk_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sRomD_h | I | I_21064A.SPI | FIN |
| sRomOE_l | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sysClkOut1_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sysClkOut1_l | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sysClkOut2_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sysClkOut2_l | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| tagadrP_h | I | I_21064A.SPI | FIN |
| tagadr_h<33:18> | I | I_21064A.SPI | FIN |
| tagCEOE_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| tagCtlD_h | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| tagCtlP_h | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| tagCtlS_h | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| tagCtlV_h | I/O | B_21064A.SPI | FDRVB_WC, FDRVB_BC |
| tagCtlWE_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| tagOk_l | I | I_21064A.SPI | FIN |
| tagOk_h | I | I_21064A.SPI | FIN |
| testClkin_h | I | I_21064A.SPI | FIN |
| testClkin_l | I | I_21064A.SPI | FIN |
| triState_l | I | I_21064A.SPI | FIN |
| holdReq_h | I | I_21064A.SPI | FIN |
| irq_h<5:0> | I | I_21064A.SPI | FIN |
| resetSClk_h | I | I_21064A.SPI | FIN |
| lockFlag_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| lockWE_h | O | O_21064A.SPI | FDRVO_WC, FDRVO_BC |
| sysClkDiv_h | I | I_21064A.SPI | FIN |
| vRef | I | Model not provided[2] | Subcircuits not provided |

[1] eclOut_h is an unused pin and should be connected to Vss.

[2] vRef should be connected to 1.4 V.

## 1.2 Alpha 21066 and Alpha 21068 Microprocessors Pin-to-Model Reference Table

Table 1–2 lists all the pins and the corresponding Level 3 SPICE models to use for the Alpha 21066 and Alpha 21068 microprocessors. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 3.00 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 3.60 V with a temperature of 25°C.

**Table 1–2 Alpha 21066 and Alpha 21068 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | **Memory Controller Pins (119 Total)** | | |
| mem_data<63:0> | I/O | T5_21066.SPI | LDRT5_WC, LDRT5_BC |
| mem_ecc<7:0> | I/O | T3_21066.SPI | LDRT3_WC, LDRT3_BC |
| mem_addr<11:0> | O | B3_21066.SPI | LDRB3_WC, LDRB3_BC |
| mem_write_l | O | U2_21066.SPI | LDRU2_WC, LDRU2_BC |
| mem_rasa_l<3:0> | O | U4_21066.SPI | LDRU4_WC, LDRU4_BC |
| mem_rasb_l<3:0> | O | U4_21066.SPI | LDRU4_WC, LDRU4_BC |
| mem_cas_l | O | U2_21066.SPI | LDRU2_WC, LDRU2_BC |
| mem_dtoe_l | O | U4_21066.SPI | LDRU4_WC, LDRU4_BC |
| mem_dsf | O | U4_21066.SPI | LDRU4_WC, LDRU4_BC |
| mem_rd_oe | O | D2_21066.SPI | LDRD2_WC, LDRD2_BC |
| mem_wr_oe_l | O | U2_21066.SPI | LDRU2_WC, LDRU2_BC |
| bc_tag<7:0> | I/O | T3_21066.SPI | LDRT3_WC, LDRT3_BC |
| bc_parity | I/O | T3_21066.SPI | LDRT3_WC, LDRT3_BC |
| bc_index | O | B3_21066.SPI | LDRB3_WC, LDRB3_BC |
| bc_idx_tag<4:0> | I/O | T3_21066.SPI | LDRT3_WC, LDRT3_BC |
| bc_cs_l | O | U2_21066.SPI | LDRU2_WC, LDRU2_BC |
| bc_we_l | O | O2_21066.SPI | LDRO2_WC, LDRO2_BC |
| bc_oe_l | O | O2_21066.SPI | LDRO2_WC, LDRO2_BC |
| bc_dirty | I/O | T3_21066.SPI | LDRT3_WC, LDRT3_BC |
| vframe_l | I | I_21066.SPI | LIN |
| vrefresh_l | I | I_21066.SPI | LIN |

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**Table 1–2 (Cont.) Alpha 21066 and Alpha 21068 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | | **PCI Bus Signal Pins (50 Total)** | |
| ad<31:0> | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| c_be_l<3:0> | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| frame_l | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| trdly | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| irdyl | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| stop_l | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| par | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| perr_l | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| devsel_l | I/O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| req_l | O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| gnt_l | I | I_21066.SPI | LIN |
| rst_l | O | B1_21066.SPI | LDRB1_WC, LDRB1_BC |
| lock_l | I | I_21066.SPI | LIN |
| pci_clk_in | I | I_21066.SPI | LIN |
| memreq_l | I | I_21066.SPI | LIN |
| memack_l | O | O4_21066.SPI | LDRO4_WC, LDRO4_BC |
| | | **Clock Pins (8 Total)** | |
| pll_clk_in | I | Model not provided | Subcircuit not provided |
| pll_clk_in_l | I | Model not provided | Subcircuit not provided |
| pll_bypass | I | Model not provided | Subcircuit not provided |
| pll_i_ref | I | Model not provided | Subcircuit not provided |
| pll_filter | I | Model not provided | Subcircuit not provided |
| pll_5v | I | Model not provided | Subcircuit not provided |
| test_clk_out | O | O5_21066.SPI | LDRO5_WC, LDRO5_BC |
| reset_in_l | I | I_21066.SPI | LIN |
| | | **JTAG Pins (5 Total)** | |
| tdi | I | IU_21066.SPI | LINU_WC, LINU_BC |
| tdo | O | O5_21066.SPI | LDRO5_WC, LDRO5_BC |
| tms | I | IU_21066.SPI | LINU_WC, LINU_BC |
| tck | I | ID_21066.SPI | LIND_WC, LIND_BC |
| trst_l | I | IU_21066.SPI | LINU_WC, LINU_BC |

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**Table 1–2 (Cont.) Alpha 21066 and Alpha 21068 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| **Interrupt, Serial ROM Interface, and instr_ref Pins (7 Total)** | | | |
| irq<2:0> | I | I_21066.SPI | LIN |
| sromoe_l | O | O5_21066.SPI | LDRO5_WC, LDRO5_BC |
| sromd | I | I_21066.SPI | LIN |
| sromclk | O | O5_21066.SPI | LDRO5_WC, LDRO5_BC |
| instr_ref | O | O2_21066.SPI | LDRO2_WC, LDRO2_BC |

## 1.3 Alpha 21164 Microprocessor Pin-to-Model Reference Table

Table 1–3 lists all the pins and the corresponding Level 3 SPICE models to use for the Alpha 21164 microprocessor. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 3.00 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 3.60 V with a temperature of 25°C.

**Table 1–3 Alpha 21164 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| addr_bus_req_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| addr_cmd_par_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| addr_h<39:4> | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| addr_res_h<2:0> | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| cack_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| cfail_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| clk_mode_h<1:0> | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| cmd_h<3:0> | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| cpu_clk_out_h | O | Model not provided[1] | Subcircuit not provided |
| dack_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| data_bus_req_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| data_check_h<15:0> | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| data_h<127:0> | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| data_ram_oe_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| data_ram_we_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| dc_ok_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| fill_error_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| fill_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| fill_id_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| fill_nocheck_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| idle_bc_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| index_h<25:4> | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| int4_valid_h<3:0> | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| irq_h<3:0> | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| mch_hlt_irq_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| osc_clk_in_h | I | C_21164.SPI | VCLK |
| osc_clk_in_l | I | C_21164.SPI | VCLK |
| perf_mon_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |

[1] cpu_clk_out_h should be left floating and not connected to etch, a voltage, or Vss.

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**Table 1–3 (Cont.) Alpha 21164 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| port_mode_h<1:0> | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| pwr_fail_irq_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| ref_clk_in_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| scache_set_h<1:0> | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| shared_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| srom_clk_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| srom_data_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| srom_oe_l | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| srom_present_l | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| st_clk_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| system_lock_flag_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| sys_clk_out1_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| sys_clk_out1_l | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| sys_clk_out2_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| sys_clk_out2_l | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| sys_mch_chk_irq_h | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| sys_reset_l | I | ID_21164.SPI | VDIN_WC, VDIN_BC |
| tag_ctl_par_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_data_h<38:20> | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_data_par_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_dirty_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_ram_oe_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_ram_we_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_shared_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tag_valid_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tck_h | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tdi_h | I | I_21164.SPI | VINB_WC, VINB_BC |
| tdo_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| temp_sense | I | Model not provided[2] | Subcircuit not provided |
| test_status_h<1:0> | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| tms_h | I | I_21164.SPI | VINB_WC, VINB_BC |
| trst_l | I/O | B_21164.SPI | VDRVB_WC, VDRVB_BC |
| victim_pending_h | O | B_21164.SPI | VDRVB_WC, VDRVB_BC |

[2] temp_sense should be left floating and not connected to etch, a voltage, or Vss.

# 2

# Reference Tables for SPICE Models of Peripheral Chips

## 2.1 DECchip 21030 PCI Graphics Accelerator Pin-to-Model Reference Table

Table 2–2 lists all the signal pins and the corresponding Level 3 SPICE models to use for the DECchip 21030 PCI Graphics Accelerator. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 4.75 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 5.25 V with a temperature of 25°C.

Each driver pin has one of four different subcircuits associated with it, as shown in Table 2–1.

**Table 2–1 Characteristics of Driver Subcircuits for the DECchip 21030**

| Subcircuits | Characteristics |
|---|---|
| GDRVA_WC, GDRVA_BC | 12 or 16 mA[1] |
| GDRVB_WC, GDRVB_BC | 4 mA with slew rate control |
| GDRVC_WC, GDRVC_BC | 4 mA, open drain output with slew rate control |
| GDRVO_WC, GDRVO_BC | 4 mA, output only with slew rate control |

[1]The value of 12 mA or 16 mA depends on whether the driver is sourcing or sinking current.

**Table 2–2 DECchip 21030 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | | **Frame Buffer Interface Pins (123 Total)** | |
| addr<17:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| addren_l<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| cas_l<3:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| casen<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| casmode<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| dsf<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| oe_l<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| ras_l<3:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| rasen_l<3:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| we_l<7:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| dacc<2:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| dacce_l<1:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| dacrw | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| data<63:0> | I/O | B4_21030.SPI | GDRVB_WC, GDRVB_BC |
| fbclk | I | I_21030.SPI | GIN |
| isce_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| romce_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| romoe_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| romwe_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| | | **PCI Interface Pins (48 Total)** | |
| ad<31:0> | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| cbe_l<3:0> | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| devsel_l | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| frame_l | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| gnt_l | I | I_21030.SPI | GIN |
| idsel | I | I_21030.SPI | GIN |
| inta_l | O | C_21030.SPI | GDRVC_WC, GDRVC_BC |
| irdy_l | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| par | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| pciclk | I | I_21030.SPI | GIN |
| req_l | O | B6_21030.SPI[1] | GDRVA_WC, GDRVA_BC |
| rst | I | I_21030.SPI | GIN |
| stop_l | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |
| trdy_l | I/O | B6_21030.SPI | GDRVA_WC, GDRVA_BC |

[1]The req_l pin, which is an output, does not use the input stage of this bidirectional subcircuit.

(continued on next page)

**Table 2–2 (Cont.) DECchip 21030 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| **Video Interface Pins (14 Total)** | | | |
| blank_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| cursor<7:0> | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| hold_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| hsync_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| toggle | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |
| vidclk | I | I_21030.SPI | GIN |
| vsync_l | O | O_21030.SPI | GDRVO_WC, GDRVO_BC |

## 2.2 DECchip 21040 PCI Ethernet LAN Controller Pin-to-Model Reference Table

Table 2–3 lists all the PCI bus interface pins and the corresponding Level 3 SPICE models to use for the DECchip 21040 PCI Ethernet LAN Controller. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 3.00 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 3.60 V with a temperature of 25°C.

**Table 2–3 DECchip 21040 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| AD<31:0> | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| C/BE_L<3:0> | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| FRAME_L | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| TRDY_L | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| IRDY_L | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| STOP_L | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| REQ_L | O | O_21040.SPI | TDRVO_WC, TDRVO_BC |
| GNT_L | I | I_21040.SPI | TIN |
| IDSEL | I | I_21040.SPI | TIN |
| DEVSEL_L | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| PAR | I/O | B_21040.SPI | TDRVB_WC, TDRVB_BC |
| INT_L | O | O_21040.SPI | TDRVO_WC, TDRVO_BC |
| CLK | I | I_21040.SPI | TIN |
| RST | I | I_21040.SPI | TIN |

## 2.3 DECchip 21050 PCI-to-PCI Bridge Pin-to-Model Reference Table

Table 2–4 lists all the signal pins and the corresponding Level 3 SPICE models to use for the DECchip 21050 PCI-to-PCI Bridge. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 4.75 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 5.25 V with a temperature of 25°C.

**Table 2–4 DECchip 21050 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| go_z | I | I_21050.SPI | BIN |
| nand_out | O | O_21050.SPI | BDRVO_WC, BDRVO_BC |
| p_ad<31:0> | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_cbe_l<3:0> | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_clk | I | I_21050.SPI | BIN |
| p_devsel_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_frame_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_gnt_l | I | I_21050.SPI | BIN |
| p_idsel | I | I_21050.SPI | BIN |
| p_irdy_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_lock_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_par | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_perr_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_req_l | O | O_21050.SPI | BDRVO_WC, BDRVO_BC |
| p_rst_l | I | I_21050.SPI | BIN |
| p_serr_l | I/O | Model not provided | Subcircuit not provided |
| p_stop_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| p_trdy_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_ad<31:0> | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_bufne_l | O | O_21050.SPI | BDRVO_WC, BDRVO_BC |
| s_cbe_l<3:0> | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_cfn_l | I | I_21050.SPI | BIN |
| s_clk | I | I_21050.SPI | BIN |
| s_clk_o<6:0> | O | C_21050.SPI | BDRVC_WC, BDRVC_BC |
| s_devsel_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_dispst_l | I | I_21050.SPI | BIN |
| s_frame_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_gnt_l<5:0> | O | O_21050.SPI | BDRVO_WC, BDRVO_BC |

(continued on next page)

**Table 2–4 (Cont.) DECchip 21050 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| s_irdy_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_lock_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_par | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_perr_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_req_l<5:0> | I | I_21050.SPI | BIN |
| s_rst_l | O | O_21050.SPI | BDRVO_WC, BDRVO_BC |
| s_serr_l | I | I_21050.SPI | BIN |
| s_stop_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |
| s_trdy_l | I/O | B_21050.SPI | BDRVB_WC, BDRVB_BC |

## 2.4 DECchip 21052 PCI-to-PCI Bridge Pin-to-Model Reference Table

Table 2–5 lists all the signal pins and the corresponding Level 3 SPICE models to use for the DECchip 21052 PCI-to-PCI Bridge. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 3.00 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 3.60 V with a temperature of 25°C.

In compliance with PCI specifications, the 21052 SPICE models include diodes to clamp overshoot on signals. You can connect the diodes to 3.00 V or 5.00 V, depending upon the desired application.

**Table 2–5 DECchip 21052 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| goz_l | I | I_21052.SPI | PBIN |
| nand_out | O | Model not provided | Subcircuit not provided |
| p_ad<31:0> | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_cbe_l<3:0> | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_clk | I | I_21052.SPI | PBIN |
| p_devsel_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_frame_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_gnt_l | I | I_21052.SPI | PBIN |
| p_idsel | I | I_21052.SPI | PBIN |
| p_irdy_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_lock_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_par | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_perr_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_req_l | I/O | B_21052.SPI[1] | PBDVB_WC, PBDVB_BC |
| p_rst_l | I | I_21052.SPI | PBIN |
| p_serr_l | OD | OD_21052.SPI | PBODB_WC, PBODB_BC |
| p_stop_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_trdy_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| p_vio | I | Model not provided | Subcircuit not provided |
| s_ad<31:0> | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_cbe_l<3:0> | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_cfn_l | I | I_21052.SPI | PBIN |
| s_clk | I | I_21052.SPI | PBIN |
| s_clk_o<4:0> | O | C_21052.SPI | PBCLK_WC, PBCLK_BC |
| s_devsel_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |

[1]The p_req_l pin, which is an output, does not use the input stage of this bidirectional subcircuit.

(continued on next page)

**Table 2–5 (Cont.) DECchip 21052 Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| s_frame_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_gnt_l<3:0> | I/O | B_21052.SPI[2] | PBDVB_WC, PBDVB_BC |
| s_irdy_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_lock_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_par | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_perr_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_req_l<3:0> | I | I_21052.SPI | PBIN |
| s_rst_l | I/O | B_21052.SPI[3] | PBDVB_WC, PBDVB_BC |
| s_serr_l | I | I_21052.SPI | PBIN |
| s_stop_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_trdy_l | I/O | B_21052.SPI | PBDVB_WC, PBDVB_BC |
| s_vio | I | Model not provided | Subcircuit not provided |

[2]The s_gnt_l<3:0> pins, which are outputs, do not use the input stage of this bidirectional subcircuit.

[3]The s_rst_l pin, which is an output, does not use the input stage of this bidirectional subcircuit.

## 2.5 DECchip 21071 and DECchip 21072 Core Logic Chipsets

The DECchip 21071 and DECchip 21072 core logic chipsets contain three types of chips: DECchip 21071–BA, DECchip 21071–CA, and DECchip 21071–DA. The DECchip 21071 chipset contains two data path chips and supports a 64-bit memory configuration; the DECchip 21072 contains four data path chips and supports a 128-bit memory configuration.

Table 2–6 lists the contents of the DECchip 21071 and DECchip 21072 core logic chipsets.

**Table 2–6 Contents of DECchip 21071 and DECchip 21072 Core Logic Chipsets**

| Chips | Function | Number of Chips for the 21071 | Number of Chips for the 21072 |
|---|---|---|---|
| DECchip 21071–BA | Data path | 2 | 4 |
| DECchip 21071–CA | Cache and memory controller | 1 | 1 |
| DECchip 21071–DA | PCI interface | 1 | 1 |

The pins of the DECchip 21071 and DECchip 21072 core logic chipsets, and which Level 3 SPICE models to use are described in Sections 2.5.1, 2.5.2, and 2.5.3. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions:

- Subcircuit names ending with WC have an operating condition of Vdd at 4.75 V with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of Vdd at 5.25 V with a temperature of 25°C.

Each driver pin has one of three different subcircuits associated with it, as shown in Table 2–7.

**Table 2–7 Characteristics of Driver Subcircuits for the DECchip 21071 and DECchip 21072 Core Logic Chipsets**

| Subcircuits | Characteristics |
|---|---|
| ADRVA_WC, ADRVA_BC | 12 or 16 mA[1] |
| ADRVB_WC, ADRVB_BC | 8 mA |
| ADRVC_WC, ADRVC_BC | 4 mA |

[1]The value of 12 mA or 16 mA depends on whether the driver is sourcing or sinking current.

## 2.5.1 DECchip 21071–BA Pin-to-Model Reference Table

Table 2–8 lists all the pins and the corresponding Level 3 SPICE models to use for the DECchip 21071–BA chip.

**Table 2–8 DECchip 21071–BA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| **CPU/Bcache Interface Signal Pins (66 Total)** | | | |
| sysData<63:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| sysPar<1:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| **Cache/Memory Data Path Control Signal Pins (13 Total)** | | | |
| sysCMD<2:0> | I | I_21071.SPI | AIN |
| subCMD<1:0> | I | I_21071.SPI | AIN |
| sysIORead | I | I_21071.SPI | AIN |
| drvSysData | I | I_21071.SPI | AIN |
| drvsysCSR | I | I_21071.SPI | AIN |
| drvMemData | I | I_21071.SPI | AIN |
| memCMD<3:1> | I | I_21071.SPI | AIN |
| sysReadOW | I | I_21071.SPI | AIN |
| **epiBus Signal Pins (46 Total)** | | | |
| epiData<31:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiBEnErr<3:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiOWSel | I | I_21071.SPI | AIN |
| epiLineSel<1:0> | I | I_21071.SPI | AIN |
| epiSelDMA | I | I_21071.SPI | AIN |
| epiFromIOB | I | I_21071.SPI | AIN |
| epiEnable<1:0> | I | I_21071.SPI | AIN |
| ioLineSel<1:0> | I | I_21071.SPI | AIN |
| epiLineInval | I | I_21071.SPI | AIN |
| **Memory Signal Pins (33 Total)** | | | |
| memData<31:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| memPar | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |

(continued on next page)

**Table 2–8 (Cont.) DECchip 21071–BA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| **Miscellaneous/Clock Signal Pins (8 Total)** | | | |
| eccMode | I | I_21071.SPI | AIN |
| WideMem | I | I_21071.SPI | AIN |
| clk1x2 | I | I_21071.SPI | AIN |
| clk2ref | I | I_21071.SPI | AIN |
| reset_l | I | I_21071.SPI | AIN |
| testMode | I | I_21071.SPI | AIN |
| tristate_l | I | I_21071.SPI | AIN |
| pTestout | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |

## 2.5.2 DECchip 21071–CA Pin-to-Model Reference Table

Table 2–9 lists all the pins and the corresponding Level 3 SPICE models to use for the DECchip 21071–CA chip.

**Table 2–9 DECchip 21071–CA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | | **CPU/Bcache Signal Pins (85 Total)** | |
| sysData<15:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| sysADR<33:5> | I | I_21071.SPI | AIN |
| tagAdr<31:17> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| tagAdrP | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| tagCtlV | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| tagCtlD | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| tagCtlP | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuCReq<2:0> | I | I_21071.SPI | AIN |
| cpuCAck<2:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuDRAck<2:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuCWMask<7:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuDWSel<1> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuDInvReq | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuHoldReq | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuHoldAck | I | I_21071.SPI | AIN |
| | | **Bcache/PAL Control Signal Pins (9 Total)** | |
| sysDOE | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysEarlyOEEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysTagOEEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysDataOEEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysDataWEEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysDataLongWE | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysTagWE | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysDatAALEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysDataAHEn | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| | | **PCI Bridge Interface Signal Pins (9 Total)** | |
| ioRequest<1:0> | I | I_21071.SPI | AIN |
| ioGrant | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| ioCmd<2:0> | I | I_21071.SPI | AIN |
| ioCAck<1:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| ioDataRdy | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |

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**Table 2–9 (Cont.) DECchip 21071–CA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| **Data Path Control Signal Pins (16 Total)** | | | |
| sysCmd<2:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| subCmdA<1:0> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| subCmdB<1:0> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| subCmdCommon | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysIORead | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| drvSysData | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| drvSysCSR | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| drvMemData | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memCMD<3:1> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| sysReadOW | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| **Memory Signal Pins (39 Total)** | | | |
| memAdr<11:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memRAS_l<8:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memRASB_l<8:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memCAS_l<3:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memWE_l<1:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memPDClk | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| memPDLoad_l | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| memPDDIn | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| **Video Support Signal Pins (4 Total)** | | | |
| vFrame_l | I | I_21071.SPI | AIN |
| vRefresh_l | I | I_21071.SPI | AIN |
| memDTOE_l | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| memDSF | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| **Miscellaneous/Clock Signal Pins (8 Total)** | | | |
| wideMem | I | I_21071.SPI | AIN |
| clk1x2 | I | I_21071.SPI | AIN |
| clk2ref | I | I_21071.SPI | AIN |
| reset_l | I | I_21071.SPI | AIN |
| testMode | I | I_21071.SPI | AIN |
| scanEnable | I | I_21071.SPI | AIN |
| tristate_l | I | I_21071.SPI | AIN |
| pTestout | I | I_21071.SPI | AIN |

### 2.5.3 DECchip 21071–DA Pin-to-Model Reference Table

Table 2–10 lists all the pins and the corresponding Level 3 SPICE models to use for the DECchip 21071–DA chip.

**Table 2–10 DECchip 21071–DA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | | **sysBus Signal Pins (52 Total)** | |
| sysAdr<33:5> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| cpuCReq<2:0> | I | I_21071.SPI | AIN |
| cpuCWMask<7:0> | I | I_21071.SPI | AIN |
| cpuHoldAck | I | I_21071.SPI | AIN |
| ioCmd<2:0> | I/O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| ioCAck<1:0> | I | I_21071.SPI | AIN |
| ioDataRdy | I | I_21071.SPI | AIN |
| ioLineSel<1:0> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| ioRequest<1:0> | O | B8_21071.SPI | ADRVB_WC, ADRVB_BC |
| ioGrant | I | I_21071.SPI | AIN |
| | | **PCI Signal Pins (47 Total)** | |
| AD<31:0> | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| CBE_l<3:0> | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| Par | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| FrameL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| TrdyL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| IrdyL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| StopL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| PerrL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| LockL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| DevselL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| ReqL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| GntL | I/O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |
| pClk | I | I_21071.SPI | AIN |
| | | **PCI Sideband Signal Pins (2 Total)** | |
| MemReql | I | I_21071.SPI | AIN |
| MemAckl | O | B6_21071.SPI | ADRVA_WC, ADRVA_BC |

(continued on next page)

**Table 2–10 (Cont.) DECchip 21071–DA Pins with Corresponding Models**

| Pin Name | Pin Type | File Name of Model | Model Subcircuits |
|---|---|---|---|
| | | **epiBus Signal Pins (46 Total)** | |
| epiData<31:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiBEnErr<3:0> | I/O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiOWSel | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiLineSel<1:0> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiSelDMA | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiFromIOB | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiEnable<3:0> | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| epiLineInval | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| | | **Miscellaneous/Clock Signal Pins (4 Total)** | |
| intHw0 | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| resetL | I | I_21071.SPI | AIN |
| clk1x2 | I | I_21071.SPI | AIN |
| clk2ref | I | I_21071.SPI | AIN |
| | | **Test Signal Pins (4 Total)** | |
| PTestOut | O | B4_21071.SPI | ADRVC_WC, ADRVC_BC |
| Tristate_l | I | I_21071.SPI | AIN |
| testMode | I | I_21071.SPI | AIN |
| scanEn | I | I_21071.SPI | AIN |

# A

# Technical Support and Ordering Information

This appendix describes how to obtain information and technical support, and order products and associated literature.

## Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

| | |
|---|---|
| United States and Canada | **1–800–332–2717** |
| Outside North America | **+1–508–628–4760** |

## Ordering Digital Semiconductor Products

To order Alpha microprocessors, peripheral chips, and evaluation boards, contact your local distributor. You can order the following semiconductor products from Digital:

### Microprocessor and Peripheral Chips

| Product | Order Number |
|---|---|
| DECchip 21030 PCI Graphics Accelerator | 21030–AA |
| DECchip 21040 Ethernet LAN Controller for PCI | 21040–AA |
| DECchip 21050 PCI-to-PCI Bridge | 21050–AA |
| DECchip 21052 PCI-to-PCI Bridge | 21052–AA |
| DECchip 21071 Core Logic Chipset | 21071–AA |
| DECchip 21072 Core Logic Chipset | 21072–AA |
| Alpha 21064A-233 Microprocessor | 21064–BB |
| Alpha 21064A-275 Microprocessor | 21064–DB |
| Alpha 21066-166 Microprocessor | 21066–AA |
| Alpha 21066A-100 Microprocessor | 21066–CB |
| Alpha 21066A-233 Microprocessor | 21066–AB |
| Alpha 21164-266 Microprocessor | 21164–AA |
| Alpha 21164-300 Microprocessor | 21164–BA |

### Evaluation Board Kits

Evaluation board kits include a complete design kit, Windows NT installation kit, and an accessories kit with an evaluation board.

| Product | Order Number |
|---|---|
| Alpha 21066A Evaluation Board Kit –233 MHz | 21A03–03 |
| AlphaPC64 Evaluation Board Kit –275 MHz | 21A02–03 |
| Alpha 21164 Evaluation Board Kit –266 MHz | 21A04–01 |
| EB30-8, DECchip 21030 Evaluation Board Kit | 21A30–01 |
| DECchip 21040 Evaluation Board Kit | 21A40–01 |
| Quad DECchip 21040 Evaluation Board Kit | 21A40–02 |
| DECchip 21050 Evaluation Board Kit | 21A50–01 |
| DECchip 21052 Evaluation Board Kit | 21A52–01 |

### Design Kits

Design kits include full documentation and schematics. They do not include evaluation boards or related hardware.

| Product | Order Number |
|---|---|
| Alpha 21064 Evaluation Board Design Kit | QR–21A01–13 |
| AlphaPC64 Evaluation Board Design Kit | QR–21A02–13 |
| Alpha 21066A Evaluation Board Design Kit | QR–21A03–13 |
| Alpha 21164 Evaluation Board Design Kit | QR–21A04–11 |
| EB30-8 Evaluation Board Design Kit | QR–21A30–11 |
| DECchip 21040 Design Kit | QR–21A40–11 |
| DECchip 21040 Quad Design Kit for PCI | QR–21A40–12 |
| DECchip 21052 Design Kit | QR–21A52–11 |

### Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

| Title | Order Number |
|---|---|
| Alpha Architecture Reference Manual[1] | EY–L520E–DP–YCH |
| DECchip 21064 and DECchip 21064A Alpha AXP PCI Evaluation Board User's Guide | EC–N0640–72 |
| Alpha 21064 and Alpha 21064A Microprocessors Hardware Reference Manual | EC–Q9ZUB–TE |
| Alpha 21164 Microprocessor Hardware Reference Manual | EC–QAEQB–TE |
| Alpha 21066, 21066A, and 21068 Microprocessors Hardware Reference Manual | EC–QC4GA–TE |
| Alpha 21066/21066A Microprocessors Data Sheet | EC–QC4HA–TE |

[1]To order and purchase the *Alpha Architecture Reference Manual*, call **1–800–DIGITAL** from the U.S. or Canada, or contact your local Digital office or technical or reference bookstore where Digital Press books are distributed by Prentice Hall.

| Title | Order Number |
|---|---|
| Alpha 21066A Microprocessor Evaluation Board (EB66+) User's Guide | EC–QDVCB–TE |
| Alpha 21066A Microprocessor Evaluation Board (EB66+) Product Brief | EC–QDVEA–TE |
| AlphaPC64 Evaluation Board Product Brief | EC–QEZMC–TE |
| AlphaPC64 Evaluation Board User's Guide | EC–QGY2C–TE |
| Alpha Microprocessors Evaluation Board Debug Monitor User's Guide | EC–QHUVB–TE |
| Alpha Microprocessors Evaluation Board Software Design Tools User's Guide | EC–QHUWA–TE |